



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/777,368

02/12/2004

Andrew J. Ritz

MS306248.1/MSFTP553US

5086

27195

7590

03/30/2007

AMIN, TUROCY & CALVIN, LLP

24TH FLOOR, NATIONAL CITY CENTER

1900 EAST NINTH STREET

CLEVELAND, OH 44114

EXAMINER

LEE, CHUN KUAN

ART UNIT

PAPER NUMBER

2181

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
--	-----------	---------------

3 MONTHS

03/30/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/777,368	Applicant(s) RITZ ET AL.	
	Examiner Chun-Kuan (Mike) Lee	Art Unit 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 7-17 and 19-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-17 and 19-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments filed 12/21/2006 have been fully considered but they are not persuasive. Rejections of claims 10, 11 and 16 under 35 U.S.C. 112 second paragraph are withdrawn. Rejections of claims 1-5, 7-16 and 21-22 under 35 U.S.C. 101 are withdrawn. Currently, claims 6 and 18 are canceled, and claims 1-5, 7-17 and 19-22 are pending for examination.

2. Regarding the withdrawal of the rejections to claims 1-5, 7-16 and 21-22 under 35 U.S.C. 101, the examiner withdraws the rejections due to applicant's amendments to each corresponding independent claims 1, 14 and 21-22, by including "embodied on a computer readable medium," rather than due to that software code along is statutory subject matter.

As stated in the preceding Final Office Action, the Federal Circuit in *Eolas Techs., Inc. v. Microsoft Corp.* establishes that "software code along qualifies as an invention eligible for patenting under these categories, at least as processes;" therefore, the software code along is statutory subject matter only if the claim is a method claim with steps that are accomplished with software routines (i.e. process). Furthermore, in accordance to MPEP 2106.01 (I):

"... computer programs claimed as computer listings per se, i.e., the descriptions or expressions of the programs, are not physical "things." They are neither

Art Unit: 2181

computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program's functionality to be realized..."

In conclusion, the examiner withdrawn the rejection of claims 1-5, 7-16 and 21-22 under 35 U.S.C. 101 because the applicant's amendment the corresponding independent claims to include "embodied on a computer readable medium," and not because software code along is statutory subject matter, as applicant argued.

3. In responding to applicant's arguments regarding the rejection of independent claims 1, 14, 17, 21 and 22 under 35 U.S.C. 103(a) that Safranek and Kondratiev fail to teach/suggest every claimed limitations; more specifically, the combined references do not teach the claimed access attribute providing both allowed and disallowed access information including access type within a single field, thus enabling allowed and disallowed control information to be stored together as well as providing both types of information for a single device, as stated on page 16, ll. 21-26. Applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that the features upon which applicant relies (i.e., access attribute providing both allowed and disallowed access information including access type within a single field) are not recited in the rejected independent claims 1, 14, 17, 21 and 22. Although the claims are interpreted in light of the specification, limitations from the

Art Unit: 2181

specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

4. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

II. INFORMATION CONCERNING DRAWINGS

Drawings

5. The applicant's drawings submitted are acceptable for examination purposes.

III. OBJECTIONS TO THE CLAIMS

Claim Objections

6. Claim 13 is objected to because of the following informalities:
in claim 13, line 3, "[0]" at the end of the claim should be deleted.
Appropriate correction is required.

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2181

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-5, 7-17 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Safranek et al. (US Pub 2004/0193755) in view of Kondratiev et al. (US Patent 6,922,740).

8. As per claim 1, 14, 17 and 21-22, Safranek teaches a direct memory access memory corruption detection system and method embodied in a computer readable medium comprising the following computable executable components:

receiving a request for a direct memory access transaction, the request comprising a least one memory address ([0014]-[0021]);

a memory controller (northbridge 117 of Fig. 1) that includes an access table (access data) that stores access information (access information stored in NoDMA table 103 and NoDMA cache 109 of Fig. 1) associated with memory (Fig. 1, ref. 101),

the memory controller employs the access information and the request to determine whether the requested direct memory access is permitted and rejects the requested direct memory access if it is not permitted ([0014]-[0016]); and

a data field comprising a corrected platform error event ([0034] and [0038]), the corrected platform error event being based, at least in part, upon a determination that a requested direct memory access is not permitted ([0034] and [0038]), the determination

Art Unit: 2181

being based, at least in part, upon access information stored in an access table (NoDMA table cache in Fig. 3) and the requested direct memory access ([0011]-[0021]).

Safranek does not teach the direct memory access memory corruption detection system and method comprising:

wherein the request further comprising a source identifier and a transaction access attribute;

wherein the access information comprising at least one source identifier, at least one memory address and at least one access attribute, the at least one access attribute distinguished from among two of read, read and write, write, and no access to indicate a combination of source and memory range identified by the at least one source identifier and the at least one memory address; and

a device driver that programs a device for a direct memory access operation, and, provides the access information to the memory controller via a direct memory access application interface.

Kondratiev teaches a system and a method comprising:

an access control list (ACL) (Fig. 2, ref. 210) (i.e. access table), the access table comprising a device ID (i.e. source identifier field), and an access attribute having a read access with memory address range and an write access with memory address range, wherein the read and write access (e.g. two distinguished access) are directly correspond to the device ID, as the read and write access indicates if the corresponding device ID will be granted/denied access to corresponding memory range (Fig. 2 and col. 4, ll. 40-65);

wherein the device ID being associated with a device (I/O device 140-1 of Fig. 1 and device ID of Fig. 2); and

a bus master (i.e. device driver) that programs (program by invoking a function to request DMA access) the device for the direct memory access operation, and provides the access information to the memory controller via the direct memory access application interface (col. 4, ll. 6-26 and col. 6, ll. 43-53).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kondratiev's device ID, read and write access attribute with memory address range and the bus master into Safranek's DMA memory corruption detection system. The resulting combination of the references further teaches the DMA memory corruption detection system comprising

the request further including the device ID and the read and write access attribute;

wherein the access information including the device ID and the access attribute having the read access with memory range and the write access with memory range, therefore the access attributes have two distinguished accesses (e.g. read and write) that directly corresponds to the device ID, as the two distinguished access indicates if the corresponding device ID will be granted/denied access to the corresponding memory range (e.g. memory address); and

a bus master that invoking the function to request DMA access for the device for the direct memory access operation, and provides the access information to the memory controller via the direct memory access application interface.

Therefore, it would have been obvious to combine Kondratiev with Safranek for the benefit of increase security and reliability for accessing DMA (Kondratiev, col. 7, ll. 30-41).

9. As per claims 2-3, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Kondratiev further teaches the direct memory access memory corruption detection system comprising the access information comprising a direct memory access request, and wherein the direct memory access request comprising a transaction type (e.g. read-write access) (Kondratiev, Fig. 2 and col. 4, ll. 23-26).

10. As per claims 4-5, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Kondratiev further teaches the direct memory access memory corruption detection system comprising the direct memory access request comprising a source identifier (e.g. device ID), and wherein the source identifier being associated with a device (I/O device 140-1 of Fig. 1 and device ID of Fig. 2) (Kondratiev, col. 4, ll. 40-65).

11. As per claim 7, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the access information comprising at least one permitted memory address (Safranek, [0014] and [0021]), wherein certain

Art Unit: 2181

segments of the memory do not have access restriction, therefore request for access are allowed.

12. As per claim 8, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the access information comprising at least one disallowed memory address (Safranek, [0014] and [0021]), wherein certain segments of the memory have access restriction, therefore request for access are denied.

13. As per claim 9, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the request comprising a read action or a write action (Safranek, [0015]).

14. As per claim 10, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the request comprising a peripheral component interface express bus transaction (Safranek, [0017] and [0019]).

15. As per claim 11, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory

corruption detection system comprising wherein the memory controller coupled to a device through a peripheral component interface express bus, the device providing the request (Safranek, [0017] and [0019]).

16. As per claim 12, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the memory controller further providing error information, if the requested direct memory access is not permitted (Safranek, Fig. 4; [0034] and [0038]), wherein the error is logged and can be utilized for subsequent analyzing.

17. As per claim 13, Safranek and Kondratiev teach all the limitation of claim 12 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising the error information comprising source information associated with the requested direct memory access (Safranek, Fig. 4; [0034] and [0038]).

18. As per claim 15, Safranek and Kondratiev teach all the limitations of claim 14 as discussed above, where Kondratiev further teaches the direct memory access memory corruption detection system further comprising the stored access information comprising a range of physical memory (access range), a source identifier (device ID), and an access attribute (read and write) (Kondratiev, Fig. 2).

19. As per claim 16, Safranek and Kondratiev teach all the limitations of claim 14 as discussed above, where Safranek teaches the direct memory access memory corruption detection system comprising wherein the request comprising a peripheral component interface express bus transaction (Safranek, [0017] and [0019]).

20. As per claim 19, Safranek and Kondratiev teach all the limitations of claim 17 as discussed above, where Kondratiev further teaches the method that facilitates detection of direct memory access memory corruption comprising storing access information in a access data store, the access information comprising a source identifier (device ID), at least one memory address (access range) and an access attribute (read and write) (Kondratiev, ACL 210 Fig. 2).

21. As per claim 20, Safranek and Kondratiev teach all the limitations of claim 17 as discussed above, where Safranek further teaches the method that facilitates detection of direct memory access memory corruption comprising a computer readable medium having stored thereon computer executable instructions for carrying out the method (Safranek, [0039]).

IV. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i):

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-5, 7-17 and 19-22 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

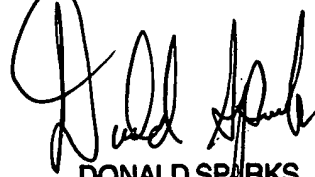
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2181

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

March 26, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

A handwritten signature in black ink, appearing to read 'Donald Sparks', is written over the printed name.

DONALD SPARKS
SUPERVISORY PATENT EXAMINER